Muhammad Anisur Rahman
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Looking for a position in any of the following disciplines
Compiler Design Engineer
Test Automation Engineer
Artificial Intelligence Engineer LLM development
AI assisted Code Generation Engineer
Electrical/Electronics Engineering
Embedded Software Engineer
Firmware Engineering
FPGA/RTL Engineering Digital and Analog , Mixed Signal design Engineer
Project Manager
Pre and Post Silicon Validation Engineer
Firmware Validation Engineer
HW SW Integration Engineer
BSP development Engineer
RTL,C modeling of hardware IP Engineer
Visual Studio,Win32 SDK ,GUI development Engineer
Hardware Validation Engineer.

EDUCATION:
Phd in Computer Science, Ls Salle University,Mandeville,Lousiana, 1999
MS in Computer Science,New Jersey Institute of Technology, Newark NJ, 1991
MS in Electrical And Electronics Engineering , University of Rajshahi, Bangladesh,1985
BS in Electrical And Electronics Engineering , University of Rajshahi, Bangladesh,1983

SUMMARY:
*AI agentic tools for C and Verilog RTL code generation.
*Claude Code , Open AI Codex.
*VS Code,Ollama, LLM AI models gemma4,Opus,Sonnet,ChatGPT 5.4 , Microsoft Copilot,Power Shell,GIT repo, Antigravity.
*Machine Learning, Image recognition
*Image fusion from multiple cameras and capturing sounds from multiple microphones.
*Embedded Linux kernel,kernel mode device driver experience. Core dump /kernel panic analysis and debug.
*Embedded Linux BSP bring up experience on various processor boards, with Multi-core SMP boot.
*Embedded Diagnostics Engineering experience.
*Embedded connectivity with I2C, MDIO,SPI,SERDES,CAN,RS232,SMBUS
*Software/firmware development for networking product such as routers, switches, DSL and cable modems .
*C , assembly programming
*Board Support Package, board bring up, diagnostics experience.
including BSP on Xilinx FPGA boards.

*Worked on various RTOS and Embedded OS such as VxWorks ,Nucleus,QNX,Linux
*802.11 wireless router Access Point (AP) software development with AAA/EAP Radius Server Authentication.Wifi MAC Driver changes to fit custom needs.
* BlueTooth Low Energy , NFC.
* Digital Signal Processing(DSP) Filter (FIR,FFT) programming in C , on digitized analog data from sensors.
*Serial peripheral protocols and device drivers experience such as I2C, SmBus, SPI, RS232, RS485,MDIO, USB etc
*Analog, Digital and Mixed signal circuit design and production experience
*TCP/IP L2,L3 PROTOCOL.
*Linux application programming experience, use of forks,threads,rpc,shared memory, client, server, C++ 11/14/17 etc
*Bare Metal (No OS) firmware development on various Controllers such as AVR32, ATmega128, 8051, 6808,68000, MicroBlaze, ARM, MIPS3000/4000, RISC V.
*Hardware Product Architecture, Embedded Firmware Architecture, Software Application Architecture, UI Application Architecture development.
Verilog RTL/SystemVerilog DPI coding for various IP such as Serial controller, Timer, DMA , RTL ,GPIO, MDIO, interface to AHB Lite bus to ARM core, Power PC bus interface. Used Synopsis VCS, ModelSim, Synopsis Verdi, Vivado,ISE,AXI_interconnect.
*Windows C/C++ programming with Win32/64SDK , MFC, Visual Studio, Windows Kernel Drivers development and debugging, trace log analysis, Crash Dump Analysis,Multi-threading, GUI App development,, C++ 11/14/17 .
*Pre-silicon SOC verification on FPGA using , C, Assembly and Verilog code.
*Post-silicon SOC verification using C, Assembly
*C modeling of Digital Systems , such as L2 switch , 64 Bit processor core control, MMU,Interrupt Controller, Battery Charging Unit, Cache Manager, Memory Controller, SRAM, Chip select, Data line, Control signal MUX for on chip peripherals in the SOC, BUS Controller, DMA Controller. System C ,System Verilog
*Well versed in Schecmatic editing. Used Orcad . Supervised Layout, Parts procurement,Mechanical Design and Manufacturing. Used Solidworks for 3D Mechanical modeling.
*Analog and Digital product design from inception to manufacturing.
*Experience in design and development of small device user and system interfaces using LCDs, keypad button.
*Hands on experience of design circuits with POWER ELECTRONICS DEVICES, MSOFET,IGBT,SCR,SHOTTKEY,HBRIDGE drivers, DC to Sine wave generation, DC-DC , DC-AC converters. Advanced Harmonics Filters. DC to 3 Phase 440 VOLT AC generation. Pspice Simulation.
*SVN,GIT,TFS,CLEAR CASE
*Compiler Design back end flow analysis with assembly code generation RBT256 processor instruction set.
*VLSI RTL Front End design experience (Specification,High level Design,Low level Design,RTL coding,Functional Verification)
*Battery charge management hardware and software development experience for different kind of batteries(Lead Acid, NiCad,Lithium Ion).

*TURBO PASCAL programming. Used RCORDS, ARRAYS, LINK LIST, STACK, QUEUE, SORTING , B-TREE , FILE/IO and other features.
*Experienced in Lab Equipment: Oscilloscope, Multi-meter,Logic Analyzers, RS232 Analyzer, I2C analyzer, Can read schematics,register color codes. Solder/De solder electronic parts on the PCB.
*Worked with various Storage protocols and File Systems - ATA, SATA, NVME, FAT16 , FAT 32, Linux EXT-2, network attached storage, Implemented Open/close/dir/close/seek/read/write/etc file system calls over the TCP/IP network.
*Experienced in MySQL , Apache, PHP, HTML5
*Windows Kernel Internals , Windows Kernel Device drivers
*Experienced in GIT CI/CD process.
*Experienced in C compiler code, proprietary parsing and IR generation and optimization and target processor assembly language generation.
*LABTOOLS - Hands on experience using various packet sniffers such Wireshark, Chamelion, AXIA, TEKTRONIX ,Logic Analyzers, Volt/Current/OHM meters. I2C analyzers, JTAG debuggers,RS232 analyzers, SPECTRUM Analyzers, OSCILLOSCOPES. SMU Keithley Instruments Inc., Model 2636A, NI-MAX , NI-VISA,Santec TSL-570 Tunable LASER generator , LabView

*Experienced in writing drivers for Network Interface (NIC) Controllers for VxWorks and Embedded Linux
*Wrote diagnostics CLI program for Beaglebone Enhanced board, configured GPIO pins, uEnv.txt, C , Linux
*Used YOCTO
*Used QEMU for ARM emulation.
*Bringup ZCU670 RfSoc based RF power controller board,VIVADO,Petalinux,C.
*NVMe over PCIe Protocols for SSD drive.

TRAININGS
*Learning AI tools for code generation. Claude code,OpenAI-Codex AI tool. VS Code,Ollama, LLM AI models gemma4,Opus,Sonnet,ChatGPT 5.4 , Microsoft Copilot,Power Shell,GIT repo, Antigravity.
*Generate C code and build the project and debug both for gcc and Visual Studio 2022.
*Generate Verilog RTL and System Verilog RTL code and simulate in Modelsim and verify the accuracy of the code generated waveform.
*Learning to create a project plan and iterate modify the Prompts until the desired output is generated by Codex and Claude code
*Learning how to write an LLM AI model from scratch,Transformer,Data input tokenizer byte pair encoding,PyTorch, token embedding ,position embedding in Vector table,Attention mechanism,Model Context Protocol
*Machine Learning, Image Recognition,DNN

Compiler Design: Developed full compiler tool chain for a new ISA architecture. I call it kcpp (Kamranga C++) .It compiles with K&R C grammar and C++9x standard. Wrote lexer,symbol table,three address code generation,basic blocks, variable interference determination, variable live ranges,color graph register allocation , assembly language generation. Object file format,executable file format,assmbler,linker,archiver,hex file generator, binary to verilog memory file. All written in Microsoft Visual C.

I wrote an Interpretive language called internetCPP (icpp), copyrighted in my name, to be embedded in HTML file. To be downloaded from **www.chapai.ai** soon, I will work on web page soon. Icpp can create llm model for learning the bytepair encoding to llm training. Icpp works with apache, it can model FPGA, simulate and synthesize using my own written verilog simulator(I call it trsim.exe -> Tuwa RTL simulator) and use icpp script for verification. One stop place for small size digital design projects.
My own designed 64 bit microprocessor runs my own designed operating system called TUWA (copyrighted in my name) compiled by my own desiged C/C++ compiler kcpp. All of them run on a Xilinx FPGA eval board. I wrote database engine called IntenetSQL (copyrighted in my name) works with C/C++,Visual Basic,PHP,icpp scripts,apache. IntenetSQL supports face and finger print recognition as well as full ANSI SQL grammar and legacy Dbase commands supports to integrate many platform into kcpp,icpp,isql-AI,trsim,iwebserver,apache hook.

Disclaimer: To make the resume short some employments are not shown here and employment dates are approximated close to the dates of employment

[AI Software Engineer Optical Test Automation , HASTEST Inc, San Jose, CA, March 2026 - present]
***Automating Entire test infrastructure for Laser based optical semiconductor test system with python code using OpenAI Codex for Global Foundry's optical chip testing**
***Python Script manages controlling SMU Keithley Instruments Inc., Model 2636A,**

Santec TSL-570 Tunable LASER generator , VIAVI Optical Power Meter (OPM),VIAVI OPTICAL SWITCH, VIAVI OPTICAL POWER AMPLIFIER and HASTEST Environmental Chamber for temperature and Humidity control.

SCPI

Keithley TSP

Modbus TCP

HTTP REST APIs

WAMP/WebSocket

TCP/IP Socket Programming

protocols for communicating with Environmental Chamber
***Plan based AI development using Codex Agentic tool**

[Software Engineer AI , ChapAI Systems Inc, Fremont, CA, November 2024 - March 2026]
*Refactoring and re-coding C code for C compiler back-end code generation tools.
*Using Claude code,Codex from OpenAI . Opus,Sonnet,ChatGPT 5.4.
*Comparing differences in C codes generated by Claude code and Codex.

*Creating project plans and specs for different modules of the compiler tools and iterate modify the Prompts until the desired output is generated by Codex and Claude code.
*Choosing the generated C codes from these two AI tools and incorporating them to the compilers back-end tools.
*Created AI agents to verify generated opcodes in the CPU Core Verilog RTL working correctly.

[Software /Firmware Engineer, HP (Hewlett Packard) , Spring Texas . May 23 - October 2024]
*Porting Microsoft Device Firmware Update driver logic to Linux.
*Built Microsoft CFU (component firmware update) application for Linux and tested on HP USB HID device.
*C/C++ /gcc, Linux libusb /hdi_api for USB device interface.
*Visual Studio 2022, Windows Kernel Drivers
*Developed state machine framework documentation using UML diagram using LUCID CHART diagram tool.
*Exposed to UEFI capsule for bios firmware upgrade.

[Software /Firmware Engineer, Microsoft, Mountain View, CA - Aug 22- March 23]
*Developing Windows Server stress test tools for Qualcomm ARM 80 core and 128 core SOC processor for server platform. Ported maxp_v3 from linux.
*Converted GNU assembly code for Microsoft ARM assembler tools
*Comparing ARM code disassembly differences between GNU and Microsoft tools.
*Wrore WDM Windows kernel driver for data exchange for the low layer test code and the test application
*Visual Studio 2022, DDK

[Electrical/Software Engineer, Intel, Santa Clara , CA - Jan 22- Aug 22]
*Modeled CXL,PCIE transaction TLP packet transfer module for simulation CXL cosim simulation for the Endpoint CXL device simulation analyzer in C/C++,System Verilog DPI,TCP/IP client server. Packets transferred from SIMICS DML code. Modified DML code for SIMICS models. Added SIMICS objects and attributes. Wrote C code for DML interface with the packet relay subsystem. Wrote System Verilog DPI to interface the CXL requests to COSIM - Synopsis VCS tools.

[Electrical/ASIC/SOC/FPGA/RTL Engineer, Microsoft, Mountainview, CA - June 21-Dec 21]
*Verilog RTL coding for 8 Channel ADC ,sample reading for Xilinx Zynq Ultrascale MpSoc, Vivado. AXI interface,FPGA, Vivado. System Verilog, for **Hololense Camera** project. Used FPGA ILA (Integrated on chip logic analyzer) for capturing FPGA internal signals for debugging the design.
*Verilog RTL coding for 4 Channel differential ADC for micrphone Audio signal sampling ,sample reading DDR capture for Xilinx Zinq, AXI interface,FPGA, Vivado.
*Created BFM for test bench generation.
* Wrote System Verilog code for test benches.
*Trouble shoot the design on the FPGA board

[Software Engineer, Panasonic Automotive, Georgia - April 2021-June 21]
Estimate storage space needed for various applications,boot,os,maps,entertainment apps for Hypervisor environment in the FLASH file system. Used Qualcomm flash file config and other resources for this research.

[Electrical/ASIC/SOC/FPGA/RTL Engineer/Embedded Software Engineer, Inceptio Inc Fremont , CA - June 2020 - April 2021]

*Worked on the Perception software for Self driving car Point Cloud Prepossessing, Voxelizing , Clustering ,Dbscan,Object Detection, Point Piller object detection. Vitis HLS, OpenCL, Accelerators.
* Converting Lidar perception C++ codes for speed enhancement for self driving automotive. , C++ 11/14/17
* Point Cloud Preprocessing, Voxelizing , Clustering ,Dbscan,Object Detection , Etc
*Converting C/C++ algorithms to Verilog RTL using Vitis HLS.
*Used EIGEN libraries for math operations.
*C/C++ and RTL Vitis Kernels
* OpenCL, Vitis -HLS, Vivado, Petalinux, Xilinx Run Time (XRT), Zynq Ultrascale Zcu102 MpSoc board,Xilinx SDK
* Petalinux BSP Config, Device Tree, FSBL
*Lidar sensor Point Piller object detection C++ code porting for FPGA acceleration, DPU, DNN,ML
*Multi core thread run, thread affinity set,CPU_SET,CPU_ZERO,thread barrier , etc.
*Validated the generated kernel with the existing firmware.
*Used BAZEL build infrastructure to build complex make of the software system

AMD - GPU Software Engineer 2020 - 2021 (Contract Position)

Build sources of ROCm software library and test the on AMD GPU.

C/C++ , Linux

[Software Test Engineer, Abott Labs, Alameda, CA - Feb 2020-June 20]

Abbot Laboratories Diabetes Care. Testing of the hand held glucose/sugar meter. Collaborated with Development Engineers, test . Systems Engineering, and Quality to Review Software Requirements and other specifications for post silicon validation test. Investigated and reported unexpected events, issues or hardware bugs during test execution. Participated in and supported the implementation, development, enhancement, and modification of test plans covering corner cases for functional testing Executed and reviewed test strategies for embedded software requirements Executed test plans using embedded debuggers (IAR Embedded Workbench for Arm) through JTAG interface on hardware test benches. Black box functional testing. Validated the embedded firmware of the hand held glucose/sugar meter as per the specifications.

[Software Engineer, Mattson Inc Fremont , CA - Nov 2019 - Feb 2020]

*Modifying Windows UI WIN32 MFC Application to accommodate unlimited number of xml recipe to configure the semiconductor plasma etch machine,(like UV Lithography,), VisualC++ 6.0.
*Wrote VAT/Pressure device simulator, Digital Mass Flow Controller (DMFC Gas Flow Controller) ,Robot arm movement,Simulator to work with PM Simulator.
*Created Command/Response packet from these devices to work with PM.
*Modified PM code in QNX application to add device simulator connectivity, C++ 11/14/17
*SEMI ,SECS standards and protocols

[Electrical/SOC/ASIC/FPGA/RTL Verilog/Software Engineer/Embedded Firmware ,New Product Development,Chapai Systems Inc, Fremont , CA - April 2019- Nov 2019]

*Developed and simulated various Verilog IP blocks for a 64 bit processor core.
*Wrote RTL model for ON CHIP Debugger to control the 64 bit processor core such as read write to the core registers, read write to any memory locations, put the core in single step mode, halt the processor, etc and this on chip debugger is tested on the FPGA.
*Wrote System Verilog code for test benches. Used UVM libraries and methodologies for the test development.
*Wrote linker tool for the custom 64 bit processor executable.
*Combined multiple objects and library modules to produce final executable file
*Combined same name memory sections from all object and lib modules in to a larger one
*Resolving symbol addresses in the final executable image
*Creating map file from the executable file
*Writing tool to create binary file from the final executable file
*Writing tool to create disassembly of the executable file section by section.
*Verify/Modify compiler back end code generation Three address Code generation, Flow analysis graph , Basic Block, Liveness of variable , SSA , Phi functions,Flow graph Immediate Dominator analysis, Lengauer Tarjan algorithm output verify, Dominator Tree, Post Dominator tree, verify interference and color graph and register allocation.
*Created BFM for test bench generation.
*Created sram.v verilog file from the executable code to make it the memory for the simulation test bench.
*Created Vivado project for the SOC verilog RTL synthesis and verification for Zynq 7 FPGA, that will execute the code.
*Modified verilog RTL for the core to insert debug for the instruction execution.
*Defined 512 interrupt line input Interrupt controller architecture for the core with multiple priority group.
*RTL Coding the interrupt controller in verilog.
*Trouble shoot the design on the FPGA board
*MIPI CPHY ,CSI Camera Interface, for RTL coding to interface to processor bus.
*Looking into Audio DSP docs for interface to the core bus.
*Writing UART driver in C for UART verification
*Writing PWM timer driver in C for TIMER verification
*Writing GPIO driver in C for GPIO verification
*Writing Embedded connectivity with I2C driver in C for I2C verification
*Writing Battery Charger driver in C for Battery Charging Controller verification
*Used Keil MicroVision 5.2 IDE compiler tools.
*Used C , Visual Studio. Verilog,Vivado tools
*Wrote RDK applications in C for Zephyr RTOS
*Working on the WordPress form development using Elementor Pro 2.x.
*Dockers,Jama,jira
*RISCV BBL boot. Multicore boot,Device Tree modification.
*used Linux libusb /hdi_api to set and get feature report of a USB device.
*Wrote Python script to run test cases

[Firmware/Software Engineer, Philips Healthcare, Bothel Washington Feb 2019-April 2019]

*Written Firmware for the motorized tooth brush.
*Written embedded code last reset reason register information retrieval from ABOV ARM core based Micro Controller using C/C++ .
A command packet is sent from the Windows UI and the embedded code communicates back with register value.
*Written Motor run timeout timer in C/C++ to protect motor from indefinite run.
*Used Cypress pSOC creator IDE to build and debug the code,
* J-Link, J-TAG ICE
*Wrote Python script to run test cases

[Firmware Engineer, Socionext,Sunnyvale, April 2018-Jan 2019]

*Developed firmware Audio/Video capture and streaming SOC project.
*Did BSP for the multicore ARM SOC on the Xilinx Zynq 7 FPGA board
*Bring up ARM multicore core based pre-silicon SOC on the FPGA.
*Bring up and test UART device
*Bring up and test QSPI controller and driver Wrote register read/write test code and driver
*Wrote APB bus access verification for Cphy, Dphy controller IP. Wrote register read/write test code and driver for device IP.
* Wrote APB bus access verification for CSI-2 Camera controller IP. test code and driver, Wrote register read/write test code and driver for device IP.
*Wrote I3C (MIPI) device driver and test codes APB bus access. register read/write test code and driver for the device IP.
*Integrated I2S driver to the BSP.
*Built the BSP directory structure and recursive make for the entire bsp
*Built bare metal BSP
*Integrated Embedded connectivity with I2C driver , tested with TDK accelerometer/gyroscope sensor
*integrated camera output frames to usb driver to connect to pc and display video streams in the pc.
*GITHUB , SVN code upload
*C, ARM DS5, GNU, Vivado, KEIL Microvision 5.
*Zynq Ultrascale , MpSoc, zcu102,Multicore SMP boot.
*Trouble shoot the design on the FPGA board
*Validated the embedded firmware for USB3,I3C.
*Wrote Python script to run test cases

[Software Engineer, Wave Computing, Campbell, Dec 2017 – April 2018].

*Wrote code that takes text file input and convert to the file to meminit.bin vector file using existing hash and conversion algorithm.
*Download the meminit.bin to Zebu emulator
*Save the Zebu output in bin file after the execution
*Modify the output bin file in other desired formats
*Wrote C program to split LAF file according Processor Cluster ID
*Wrote C program to join multiple processor cluster INIT vectors in to one large init file for combining multiple processor cluster into one large processing machine.
*Modified Wavelib , added features to WaveLib all in C .

*Installed CUDA ,Installed Tensorflow,Installed Onnx,Installed Caffe2.
*Tried Tensorflow machine learning codes to freeze the graph and convert to Onnx.

[Electrical/ASIC/FPGA/RTL Verilog/Embedded Firmware , Renesas Inc, Santa Clara, July 2017 – Dec 2017]

*Integrating various VLSI design Verilog RTL IP to IOT controller design based on ARM m4 Core
*Ported . Verilog RTL to implement ip of DMA controller to AHB lite bus protocol of M4 Arm core. Synopsis VCS simulation , test bench for Bus functional model. Use Verdi for waveform examination. Xilinx Vivado for FPGA implementation , bit stream generation. Design tested on the FPGA board. Used IAR ARM compiler debugger to download the c program executable and debug on the board.
*Created System Verilog BFM for test bench generation.
*Soc tested on the Xilinx Zynq 7 FPGA board.
*Ported ARM Cordio BLE Wireless Bluetooth Low Energy software stack code for the FPGA board.
*Wrote LCD panel driver for AMPIRE 320x240 in Verilog RTL to write RGB pixel data to the panel Synchronized with VSYNC, HSYNC, and VCLK, VENABLE signals
*Wrote and verified GPIO IP in Verilog/System Verilog
*Modified NOC (Network on a Chip) to create the chip select and port address decode to access GPIO registers
*Ported Pin Function Select IP in Verilog.
*Ported PWM IP RTL and integrated to the ARM Bus protocol, Coded in Verilog
*Verfied QSPI interface module
*Ported and Integrated RTC module
*Wrote C code to DMA transfer data between the Blue tooth Base band controller and the host memory.
* Zync , MpSoc, zcu102,Vivado
*Trouble shoot the design on the FPGA board
*Validated the embedded firmware for BLE , Serial,QSPI drivers.
*e2studio Renesas, Renesas RA6M4 and RA6M5 board, ARM core,FreeRTOS, Azure NetxDuo,Threadx
*Wrote Python script to run test cases

[Embedded Software Engineer, Calix Inc, San Jose CA, Oct 2016 - May 2017]

*Developed Embedded software for Wireless Network Gateway.
*Implemented DCLI for IPV6 L3 Host and Route table programming for Broadcom Tomahawk switch
for the HAL – Manager
*Implemented for IPV6 L3 Host and Route table programming from FIB
to the HAL – Manager.
*Used Broadcom SDK for Tomahawk switch.
*Fixed DCLI DHCP configuration bugs.
*NETCONF protocol, YANG coding for CLI
*C, Embedded Linux, JIRA, YOCTO, SMOKE TEST
*Wrote Python script to run test cases

[Software Engineer , Mattson Inc, Fremont CA, April 2016 - Oct 2016]

*Developing code for RAW data collection and process for plotting from the Semiconductor plasma etch machine and send to the Windows UI, from QNX 6.3
*ported first order digital filtering (FIR) of the sample raw data from sensors in C.

*Developed UI using MFC and C++ ,C/C#.NET,to process control messaging for receiving raw and processed data from the process control to UI program in PC.
*Ported the digital filtering (DSP) FIR , FFT code from UI Windows side to the QNX plaform
*Developed code to display Endpoint Graph as well as generate event for the Endpoint
*Developed UI to display of the Wafer Run Lot Summary per cassette/Foup show wafer process status, RF time per step.
*Recipe Management System (RMS) ,Create, Edit, Download Receipe.
* C#,C/C++, Visual Studio,.NET, SQL MFC, WIN32/64 SDK ,multi-threading
*Modified and Enhanced Windows WDM kernel Driver for I/O card. Windows 2000 DDK, WinDbg, C, Remote Debug.
*Wrote software to communicate to the machine over RS232,RS485 communication link, Real time data acquisition with Power DAQ.
*Follow SEMI,SECS standards and protocols

[Embedded Software Engineer INTEL Inc, Santa Clara CA, Oct 2015 - April 2016]
*Wrote Post silicon test codes to test ARM A53 4 core SMP ASIC to test if multi-core thread execution is working.
*Spawned multiple ThreadEx RTOS threads of the same functions with different priorities. In the threads core id
Is being checked to determine which core is executing the code.
*Created data structures to hold results/errors per core.
*GNU C, ARM Assembly language
*ARM DS debugger. THREADX RTOS.
*SVN,GIT,TFS

[Embedded Software Diagnostics Engineer, Cisco System , San Jose CA, March 2015– Oct 2015]
Writing C programs for ASR9000 router's shock-wave RSP4-S ,FC2,LINE CARD diagnostics for Cisco ASIC and other devices.
*Serdes Loopback test, PRBS test, BIST memory test, Register test ETC, Uart Loopback, Ethernet loopback.
*Wrote kernel driver for the CAN controller;
*C , Wrote Embedded Linux, Kernel Drivers, User mode apps for diagnostics, etc
*Trouble shoot kernel drivers.
*Validated diagnostic firmware cable modem head end control and management board.
*Wrote Python script to run test cases

[Platform Software Engineer, NetApp , Sunnyvale CA, Oct 2014– Feb 2015]
Wrote C code for Platform System Health monitoring. Involved read device registers for errors and failures.
Create data tables , policy files and rules for error / warning /alert definition. Configure Auto Support etc,Worked with PCIe, NVMe Protocols for SSD drive, Fiber Channel, SAS devices.

[Embedded Software Engineer ARRIS-Motorola May 2014-OCT 2014]
Wrote / debugged embedded C programs for WiFi 802.11 a/c/n protocols for Wireless broadband router for 2.4G Broadcom and 5G 802.11acQuantenna Radios. Work involved integrating quantenna radio parameters in one single repository configuration manager. Used QCSAPI SDK for SSID configure and stats collection for 5G Quantenna radio. Modifying Quantenna QDPC host PCie driver for adding ioctl. **ARM Cortex 4 SMP core** , Embedded Linux, C.

GitHub (Git) version control, BCM6362 ,63138A ,63148A Broadcom Micro Controllers. TR-098,Fixed bugs in 595/599 models of router software. Cross compiled in Ubuntu Linux platform.
*Tested/ Validated and made changes in Cable modem WiFi router firmware for end client Comcast on behalf of Arris.
*C , Embedded Linux,Broadcom,Quantenna,,ACS, DOCSIS, ATOM,ARM
*Written API interface for RDKB
*Fixed bugs for Arris WifiWireless Cable Modem OG1600, 1682 .
*Made code changes to add RSA/AAA/ EAP RADIUS server authentication for enterprise security feature.
*Made code changes to add Primary RADIUS server failover to secondary radius server
*Made code changes to enable Disconnect request by Remote RADIUS server.
*Used YOCTO build frame work for code repo and code building for client.
*Used QEMU for ARM emulation.
*Created Yocto bb and bb append recipe files for WiFi Host AP modules.
*Wrote code to implement client station Black Listing for authentication rejection by the Radius Server.
*Configured band steering parameters.
*Modified HOSTAPD BSS configurations
*Modified 802.1x files for adding new features.
*Modified Wifi AC device driver codes on Qualcom chipset for HAL layer
*Worked with Wi-Fi -ac QCA hostapd codes.
*Modified Mac driver to fit AAA related need.
*Worked with WPA pass phrase
*Traced and generated test packets from IXIA ,Wireshark for debugging purposes
*JIRA issue tracking
*Used Lauterbach Trace32 In-Circuit Debugger. Download image , debug the program, configured the Lauterbach Trace32 script file for download and debug
*Validated the changes in the WiFi device drivers firmware.

[Embedded Software Diagnostics Engineer, Cisco System , San Jose CA, April 2012– May 2014]
Writing C programs for Cable Modem Head End (CMTS) supervisor and line card device functionality test. All coding are in the Embedded Linux platform. Intel Shumway board, cavecreek Chipset USB, PCIe, SATA, SPI etc.
Multi-threaded linux app coding, kernel mode device driver module coding,Kernel DMA driver,spinlock, MSI interrupts,tasklets,workqueue,kmalloc, linux interrupts, IO remap, Grub configuration, init scripting, SMbus driver coding,Embedded connectivity I2C driver coding, Marvel Switch 98x243 programming, makeroot,cpio,PCIedrivers,MSI interrupts,memtest86+C,gnu, Linux 2.6.39.4, INTEL Sandy bridge SMP core x86 Micro Controller.
*Trouble shoot drivers and other software developed.
*Wrote Python script to run test cases

[Embedded Software Engineer, Broadcom , San Jose CA, Sept 2011 – Jan 2012]
***Performed the Post-silicon validation**
***Wrote C programs to verify Ethernet Ethernet PHY SERDES on a new silicon,**
***Wrote low level kernel Ethernet PHY device driver for 10G/40G BROADCOM Trident Warp core Ethernet PHY silicon on a fiber optics Network Interface Card(NIC) .**

*Programmed/verified registers , bringing up Auto Negotiation IEEE CL37.
*Programmed/verified register to configure lane bandwidth 1g/5g/10g etc.
*Programmed/verified memory management registers for l2 switch operation
*CJ PAT, PRBS,BERT etc.
*C, VxWorks RTOS,Multitasking.

[Electrical/ASIC/FPGA/RTL Verilog/Software Engineer/Embedded Firmware/Design Engineer Analog/Digital, Project/Product/Program Manager, Sun Power Circuit Inc, Fremont CA, Aug 09 – Sept 2011]

*Solar Inverter Development project
*Project Manager/Product Architect /New Product Development Engineer. Architected the Solar Power Inverter including embedded firmware/software, electrical circuits, mechanical enclosure, Managed product development teams in India, China for software and hardware product development. Product architecture, specification, product power point presentation preparation. Cost estimate, work scheduling, schedule tracking , resource management.
*Architect-ed and implemented hardware and embedded firmware for the Solar Power DC to AC Inverter.
Atmel AVR ATMega128 Micro Controller AVR Studio , C , JTAGICE-MKII. Built bare metal BSP
*Used PWM, ADC interfaces ,etc.
*ATMel's ATMega128 Micro Controller, AVR32 Micro Controller Studio , C , JTAGICE-MKII.
*ST Micro's STM32 Micro Controller, NXP's LPC55S16JBD64K STM32 Micro Controller, FreeRtos
*Used PWM, ADC interfaces ,etc.
*Implemented several hardware and software blocks of the product.
*Wrote device drivers.
*Used Perforce source code control.
*Created System Verilog BFM for test bench generation.
* Developed FPGA RTL using VERILOG to program the Xilinx Spartan 3 FPGA to connect the Atmel controller to different devices.
*SystemC power modeling.
*Coded PWM timer module in VERILOG, Coded PWM Sinewave generator in VERILOG , Coded Line Frequency detector and phase sync interrupt generator in VERILOG.
*Used Modelsim for the RTL simulation. Wrote bus functional model for the test bench. Created stimulus file and expected output file. Compared RTL output to the expected out file. Prepared Test bench, and Test Cases
*Wrote System Verilog code for test benches. Used UVM libraries and methodologies for the test development.
*Used Xilinx Vivado to FPGA Synthesis place & route and bit file generation.
*Used EDA tools for schematic entry.
*Design was a mixture of analog and digital circuit blocks.
*Used pSpice for circuit simulation.
*Used MOSFET,IGBT, Gate Controlled SCRs, Ferrite Transformer,SPI Digital To Analog (DAC) and Analog to Digital (ADC) Converters. Used DAC124S085, OP AMP LM324, Embedded connectivity with I2C Devices in the design.
*Developed Board bring-up and diagnostics codes.
*Architect-ed and implemented Battery management software and hardware. Software driven PWM based, MPPTS,
Floating,boot and trickle charge system, etc. Software driven algorithm to save battery at different load level and no load level.
*Worked with AC/DC and DC/DC coverters, Buck-Boost, FlyBack, H-Bridge Circuitry, SCR, Power Electronics, Power Supply,SineWave Generation circuits and filters, DC to 3Phase 440 VOLT AC generation.

*Used Pspice simulation for different parts of circuits.

*Selected parts per specification for the schematic and simulation.
*Supervised PCB layout forhighspeed design for proper device placement, vcc and gnd plane, via, trace lengths, filter capacitor placenment, clock line, etc.
*Interacted with PCB fab houses in China.
*Travelled China to meet companies for making plastic molds, enclosure fabrication and other for manufacturing needs.
*Managed development team overseas and US.
*Solidworks2010 3d enclosure design
*Pyhton scripting for test automation
*Cross compiled in Centos 5 Linux platform.
*Tl Code Composer ,C2000
*TI Soc AM57xx Micro Controller ,C/C++
*Matlab and Simulink for modelling and simulation.
*Trouble shoot circuits boards, drivers and applications.
*Used Free-RTOS for product development
*Developed battery management system software (BMS) in C. Manage charging of the battery, over current and short circuit shut down, keep track of the temperature of the battery and charging hardware, enable the and disable the charging system as needed from PV source as well as grid,generate logs, communicate with the inverter software.

[Embedded Software Engineer , CISCO Systems, San Jose CA, Jan -2007 – Aug 2009]
*Wrote test/diagnostics for exercising switching ASICs (R2D2, Metropolis,Eureka,Lamira,Octopus, Santa Cruz, and crossbar spine) for Nexus 7000 on 1G (Nurbergring) and 10G (Albert Park) line cards. C and embedded Linux OS ,Linux device drivers. Packets are injected through in-band port of r2d2 to the full capacity of the line-card including both L2 forwarding (eureka) and L3 forwarding (lamira) look up.
*Developed software for Cisco CRS-1 router.. C/C++ , QNX ,Multi-threading. D-Bus
*Fixed and enhanced cli for CRS-1 router.
*Added new CLI features to fabric snapshot for CRS-1 router.
*Converted fabric snapshot TCL script to C for CRS-1 router.
*Rewritten fabric snapshot CLI to spawn on proper node by detecting the board type (LC, RP, Fabric,etc) for CRS-1 router.

[Embedded Software Engineer ,Aquest Systems Inc, Sunnyvale CA, March 06- May -06]
*Worked on (Automated Material Handing Systems) AMHS project for semiconductor industry, each LOAD of Wafer container is routed to different fabrication machine for etch and deposition and mask , through conveyor system and rotating table to change the direction of travel of the container based on the destination machine location intended for each container. Stepper motors were moved based on the command packets received over the Ethernet IP packets and the controller interprets the packet and apply rotation of the stepper motors.
*Developed firmware to control PMD stepper motor to move FOUPS on the conveyor, Rotating table
Used uCos-2 RTOS, Microblaze Micro controller, GNU Debugger, C/C++, Framework,Interprocess communication,MessageQueue,Semaphores.
*Validated the firmware against the functional specification for the stepper motor.

[Embedded Software Engineer ,Agere Systems Inc, SanJose CA, Jan 05- April 05]
*Wrote Post silicon test/diagnostics 48 Port Gigabit switch
*Implemented dynamic mac address aging algorithm for 48 Port Gigabit switch in the software to compensate the hardware problem to tag a mac address to be dynamic or static .
Worked on Level 7 HAPI/DAPI and Device Driver Layer integration and debug for 48 Port Gigabit switch
unsing PPC 824x CPU. VxWorks, Tornado. All developments done in C.
*Wrote Post silicon Trouble shoot for L2 MAC engine.

[Electrical/Design Engineer, NetOptics, SunnyvaleCA, Jan 04- Jan 05]
*Project Lead for Software Development.
*Architected and coded firmware and management software for next generation network traffic sniffing/security box. It is a combination of Intrusion Detection and Protection feature(IDS/IPS). Box is running embedded Linux. Coded firmware for embedded Linux and management software for windows win32 SDK. Wrote linux kernel mode device drivers etc.
Box scans emails, attachments(pdf,xls,doc,ppt,txt and more), ftp and all other payloads in the link in 10/100/gigabit speed. It remembers tcp/ip sessions, to and from ip addresses and port numbers.
Embedded software works with verilog/fpga to store all matched entries and transmit them to administrator of the box. Windows software talks to the embedded side of the box and loads all signature patterns and other required parameters needed for sniffing. A patent application has been filed on this firmware/software.
Search is done using IDT NSE (Network Search Engine) Chipset.
*Wrote low level Linux driver to connect two Gigabit Network Interface card (NIC)through the filter and matching engine. Used DMA from/to MAC layer data transfer. Wrote MDIO driver for PHY configuration. Ethernet packets were sniffed and matched in the match software hardware.
Embedded processor is the PPC405 based Micro Controller stamped in XILINX VIRTEX2-PRO FPGA.
*Wrote Dallas RTC interface in VERILOG RTL and integrated to the OPB bus IP and implemented in Xilinx EDK 6.1 and synthesized using ISE 6.1, used ModelSim simulator for RTC interface simulation. Used ChipScope Pro
Used C for all software development.
*Wrote server for connecting to the Windows GUI clients, Server forks to serve multiple GUI clients.
*Wrote driver software in C for hardware functional blocks verification in the FPGA.
*Python scripting for test case automation
*Wrote board bring-up and diagnostics codes.
*Patent approved #7499412
*Virtualized the IPS/IDS engine on the Linux platform. Virtualized Engine was developed in C.
*Used VHDL to glue CPLDs for creating chip selects for different devices

[Electrical/ASIC/FPGA/RTL Verilog/Software Engineer/Embedded Firmware Engineer, Project Manager ,CellstatInc , Palo Alto CA June 03- Dec 2003]
*Project Manager/Product Architect. Architect-ed embedded firmware /software and UI for measuring electrical response of human body cell data collection equipment for cancer research. Managed product development teams in India, Bangladesh for software and hardware development. Product architecture, specification, product power point presentation preparation. Cost estimate, work scheduling, schedule tracking , resource management.
*Designed medical research equipment for cancer research.
*Developed VERILOG FPGA RTL in Verilog for controlling relay matrix hardware and wrote software for monitoring electrical response of human body cell. Xilinx Spartan 3 FPGA is used for the design implementation..Used ModelSim for Simulation . Prepared Test bench, and Test Cases. Used Xilinx ISE tools for FPGA Synthesis place & route and bit file generation.

*Written/Modified VHDL RTL to create the state-machine that control DAQ subsystem.
*Created Verilog BFM for test bench generation.
*Integrated various Verilog RTL ip in to the current design.
*Wrote 80x86 Assembly routines to read A/D data from the the Data Acquisition Port
*Orcad Pspice for circuit simulation
*Orcard Schematic.
*Selected parts per specification for the schematic and simulation.
*Used Pspice simulation for different parts of circuits.
*Supervised PCB layout and interacted with PCB fab houses in China.
*Digital Signal filtering implemented in C on the data captured from the ADC.
*C and Assembly languages are used.
*Developed GUI using C/C++ for windows platform to control the board.
*Implemented DSP FIR,FFT ,IIR techniques to process raw digitized signal filtering after analog to digital conversion from the sensors
*SQL database development with InternetSQL server.
*Wrote device driver software in C to verify hardware functional blocks in the FPGA.
*Wrote board bringup and diagnostics BSP code for Embedded Linux (Monta Vista) .
*Customized U-Boot for booting Embedded Linux on the board.
*NXP ARM code Micro Controller
*Built bare metal BSP

|Electrical/ASIC/FPGA/RTL Verilog/Software Engineer/Embedded Firmware Engineer, Manager Program/Product development, Misk Technology Inc , Fremont CA May 2001- March 2003|

*Managed multiple projects development teams in India, Bangladesh, China for software and hardware product development. Duties were to develop product architecture, specification, product power point presentation preparation, finding and interviewing qualifying teams in India, Bangladesh, China. Cost estimate, work scheduling, schedule tracking , resource management.
*RTL design for on chip debug hardware module for state machine using VERILOG RTL.
*Developed DDR2 memory interface RTL in Verilog.
*System C,System Verilog
*Wrote System Verilog code for BFM test benches. Used UVM libraries and methodologies for the test development.
*Did VERILOG RTL coding , simulation , waveform analysis. Test bench generation in verilog. Did C modeling of the module.
*Modeled Gate Level Simulation for combinational circuits using verilog AND, NOT, OR etc gate primitives .
*Matlab and Simulink for modelling and simulation.
*Integrated various Verilog RTL ip in to the current design.
*Built bare metal BSP
* Developed bus functional models, inputs and stimulus and compare procedures for RTL verification using C and Perl language. Prepared Test Case generation.
*Used Xilinx ISE tools for FPGA Synthesis place & route, timing closure, and bit file generation.
*Developed 10/100 Emac controller for Mii interface in verilog for the processor core supporting half duplex mode.Implemented back-off algorithm on collision detection in half-duplex mode.
*Developed CPU Host Interface block for reading writing to PHY registers. Created MDIO control and data registers for host access. Drove MDIO/MDC signals.
*Developed UART controller in verilog for the processor IP. Only 9600 baud supported.
*Used Leonardo Spectrum for FPGA/ASIC Synthesis, technology library selection, etc.
*Wrote stepper motor drive logic for host bus in Verilog for RKD514LA stepper motor drive.
*Wrote software drivers for hardware design verification in C.
*Written Driver for TI RFID controller in C. Developed GUI for Device test.
*Orcad Schematic Entry.

*SQL/Mysql /Php/Html/Linux development for web based device configuration system.
*Wrote PHP interface for loading custom DLL for Apache server.
*Wrote board bring-up and diagnostics codes.
*Written firmware for Ethernet fault tolerant switch using ARM 9 ASIC . C , assembly, Embedded Linux, kernel mode device driver ,linux boot loader.
*Wrote Windows GUI and Windows Kernel Driver to configure the switch ASIC. Created I2C frame packet and transferred the packet from 2 parallel port pins of the PC to the switch board EEPROM. Also read back data from NVRAM through parallel port pins.
*Programmed Bare Metal (No OS) 8051 based controller to control Ethernet switch. C, assembly ,Keil.
* Written C code for Smart card command send/receive driver for mobile phone SIM card using CALMRISC16 microcontroller. Used CalmSHINE16Plus1 Cross Compiler tools.
*Designed 100 MHZ RF wireless transceiver to receive and transmit digital data 2 bits encoded in the phase modulation. Used Pspice , Orcad
*Developed small footprint SQL RDBMS Engine for embedded application in C++. ANSI SQL implemented .Copy right with US Library of Congress in the name "Internet SQL"

*Developed Multitasking fully blown RTOS in assembly and C and ported for MIPS 3000,4000,ARM 9 Micro Controllers and MICROBLAZE Micro Controller . Copy right with US Library of Congress in the name "TUWA RTOS"
*Converted H.264 encoding decoding C code to Verilog. Created test benches, created sample images frames data and fed the encoder and decoder.
*Developed 8b/10b SerDes in Verilog RTL and Implemented on the Xilinx FPGA
*Developed and integrated industrial communication solutions using Modbus RTU and Modbus TCP protocols for monitoring, control, and data acquisition across power systems and industrial automation platforms.
*Implemented Modbus-based communication interfaces for real-time monitoring and control of transformers, protection relays, meters, PLCs, and intelligent electronic devices (IEDs).
*Designed and debugged Modbus RTU/TCP communication stacks, including register mapping, polling mechanisms, exception handling, and protocol diagnostics for embedded and Linux-based systems.
*Performed troubleshooting and protocol analysis of Modbus networks using serial and Ethernet communication interfaces, ensuring reliable interoperability between multi-vendor industrial devices.
*Experienced with Modbus register configuration, data acquisition, device addressing, function codes, and communication performance optimization in industrial and utility environments.

*Designed and architect-ed base-band digital module , serializer and de-serializer for the 100 Mhz RF Transmit / receive unit using Verilog RTL.
*Created AHB bus integration for ARM cpu based Micro Controller for the base-band digital module. Tested on FPGA
*Wrote Windows File System device driver for Windows kernel. The file system is implemented for network attached storage device which uses EXT2 format . The File system appears in the window as a drive letter Z:
*Wrote driver to capture ADC signal from Microphone AUDIO. ADC signal was captured 8000 samples per second and put on the DMA to the host memory for further processing
*Developed automated test, monitoring, and data acquisition applications using LabVIEW for industrial control systems, electrical equipment diagnostics, and laboratory instrumentation.
*Designed LabVIEW-based applications for real-time data acquisition, signal processing, equipment control, and visualization using DAQ hardware, serial interfaces, Ethernet, GPIB, and USB-connected instruments.
*Integrated LabVIEW applications with industrial communication protocols such as Modbus, TCP/IP, and SCADA interfaces for remote monitoring and control of power system and automation equipment.
*Created automated test and validation frameworks in LabVIEW for transformer diagnostics, electrical measurements, and hardware verification, improving test repeatability and operational efficiency.

*Experienced in developing user interfaces, data logging systems, alarm handling, and report generation tools within LabVIEW environments for engineering and industrial applications.
*Utilized LabVIEW in conjunction with National Instruments hardware and instrument drivers for high-speed measurement, control, and hardware-in-the-loop (HIL) testing applications.

[Embedded Software Engineer , COPPER MOUNTAIN NETWORKS, Fremont, CA April - 2001-Aug2001]

* Written device driver for DSL line card. Written pre-activation multirate pulse driver for conexant BT8973 Micro controller for DSL chip on PowerPC 8240 (PPC 603) core. Programmed EPIC controllers. Modified bit pump codes for phase and AGC adaptation,framer modes and scrambling.BCM63268, BCM6362, BCM6368, BCM6328, DslxChange,VxWorks RTOS,Tornado. Validated the DSL modem training firmware. All developments done in C.

[Embedded Software Engineer , COM21, Milpitas, CA-June 1999 -April 2001]

*Written VxWorks BSP for MIPS 3350/3352 based on Microcontroller for Cable Modem.
*Wrote device drivers for SERIAL , USB , ETHERNET, TIMERS and more
*Wrote driver for XILINX SPARTAN FPGA configuration file downloader.
Ported broadcoms HPNA driver for broadcom 4210 iline chip for cable modem based on broadcom 3350 docsis modem chip.
*Wrote boot loader code.
*Wrote Flash and NVRAM driver for cable modem board.
*Written codes for Bridging and Filtering IP packets.
*Wrote software in C for diagnostics and hardware verification.
*C/C++, Multitasking, Inter-process communication,Message,Queue,Semaphores.
***Ported VoIP,SIP,EPTAPP,xChange software stack.**
***Programmed TI Digital Signal Processor for the digitized Audio signal filtering. FIR , FFT**
*** Worked with SLICK/SLACK,etc.**
*** Integrated AUDIO CODEC input output for IP telephony purpose**

*Modified RF tuner driver that controls AGC and other parameters of the RF communication.
*Wrote board bring up, board diagnostics , memory test codes.
*Configured DRAM memory controllers

WORK STATUS : US CITIZEN
Disclaimer: Employment dates shown are approximate and not all employments are shown in the resume.
linked in: https://www.linkedin.com/in/muhammad-rahman-2973673b/